Fact Sheet

MOTOROLA POWERPC 604E™ MICROPROCESSOR

The PowerPC 604e microprocessor is a 32-bit implementation of the PowerPC Reduced Instruction Set Computer (RISC) architecture. The PowerPC 604e microprocessor provides high levels of performance for desktop, workstation, and symmetric multiprocessing computer systems. The PowerPC 604e microprocessor is software- and bus-compatible with the PowerPC 603e™, PowerPC 740™ and PowerPC 750™ microprocessor families.

Superscalar Microprocessor

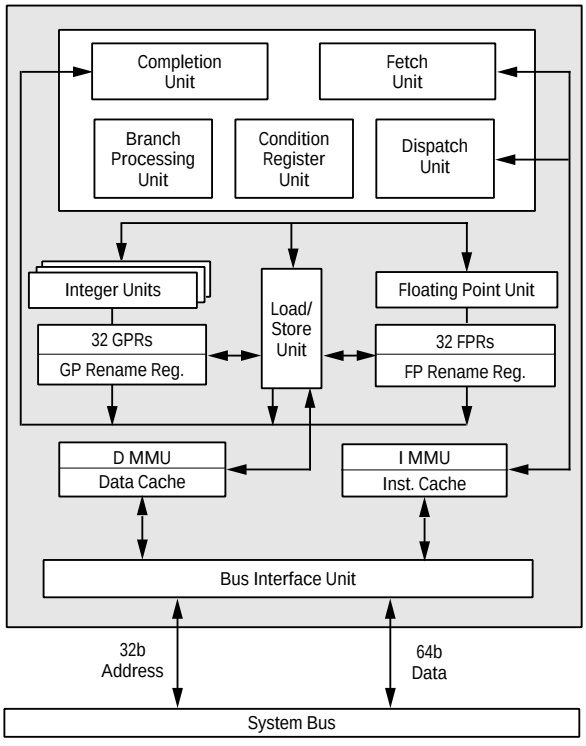
The PowerPC 604e microprocessor is a superscalar design capable of issuing four instructions per clock cycle to seven independent execution units, including:

- Two single-cycle integer units
- One multiple-cycle integer unit
- Branch processing unit
- Load/Store unit
- Floating-point unit
- Condition register unit

Instructions can execute out of order and execution results can be made immediately available to subsequent instructions through the use of rename registers. However, the completion unit retires (commits results to architectured registers such as FPRs and GPRs) as many as four instructions per clock cycle in order, ensuring a precise exception model.

The PowerPC 604e microprocessor uses dynamic branch prediction to improve the accuracy of instruction prefetching. This and the ability to speculatively execute through two unresolved branches minimize pipeline stalls.

PowerPC 604e Microprocessor Block Diagram



Cache and MMU Support

The PowerPC 604e microprocessor has separate 32-Kbyte, physically-addressed instruction and data caches. Both caches are four-way set associative and provide byte-level parity checking.

The PowerPC 604e microprocessor also has separate memory management units (MMUs) for instructions and data. The MMUs support up to 4 Petabytes (2^{52}) of virtual memory and 4 Gigabytes (2^{32}) of physical memory. Access privileges and memory protection are controlled on block and page granularities.

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Large, 128-entry translation lookaside buffers (TLBs) provide efficient physical address translation by storing the most recently used page translations.

Flexible Bus Interface

The PowerPC 604e microprocessor has a high performance 64-bit data bus and a separate 32-bit address bus. The interface protocol allows multiple masters to access system resources through a central arbiter. On-chip snooping logic maintains cache coherency in multiprocessor systems. Because the PowerPC 604e is optimized for multiprocessor systems, snooping does not require additional bus cycles.

PowerPC 604e Major Features

- Fully JTAG-compliant
- More flexible control of bus operations that can greatly improve bus-cycle time
- The PowerPC 604e provides the same hardware support for misaligned little-endian accesses as it does for big-endian accesses
- Three additional registers for increased performance monitor support
- Low power modes – doze, nap, sleep

PowerPC 604e CPU Summary

CPU	604e 180-233 MHz	604e 250-350 MHz
CPU Speeds - Internal	180, 200, 225 and 233 MHz	250, 300 and 350 MHz
CPU Bus Dividers	x2, x2.5, x3, x3.5, x4	x3, x3.5, x4, x4.5, x5, x5.5, x6, x6.5, x7
Bus Interface	64-bit data & 32-bit address	64-bit data & 32-bit address
Instructions per Clock	4	4
L1 Cache	32-Kbyte instruction 32-Kbyte data	32-Kbyte instruction 32-Kbyte data
Typical/Maximum Power Dissipation	13.5W/14.3W @ 180 MHz	6.0W/10.6W @ 250 MHz
Die Size	148 mm^2	47 mm^2
Package	255 CBGA	255 CBGA
Process	0.35µ 5LM CMOS	0.25µ 5LM CMOS
Transistors	5.1 million	5.1 million
Voltage	3.3V i/o, 2.5V internal	3.3V i/o, 1.8V internal
SPECint95 (estimated)	9.4 @ 200 MHz	14.6 @ 350 MHz
SPECfp95 (estimated)	8.7 @ 200 MHz	9.0 @ 350 MHz
Other Performance	418 MIPS @ 233 MHz	629 MIPS @ 350 MHz
Execution Units	Integer (3), Floating-point, Branch, Load/Store, Condition Register	Integer (3), Floating-point, Branch, Load/Store, Condition Register

For additional information:
call 1-800-845-6686 or your local Motorola sales representative
or visit http://motorola.com/PowerPC/

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